## REMARKS

Thus, claims 21-24 and 26 are present for examination.

Claims 21-24 and 26 stand rejected under 35 U.S.C. 112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Moreover, claims 21-24 and 26 stand rejected under 35 U.S.C. §112, second paragraph as being indefinite.

Both rejections are respectfully traversed in view of the amendments made herein:

Claims 21 has been amended to recite a method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising,

forming a plurality of field insulating films in parallel with one another in a first direction on a semiconductor substrate, each of said plurality of field insulating films provided for a plurality of memory cell transistors and a plurality of memory transistors formed between two associated adjacent field insulating films;

forming a first gate insulating film in each of active regions;

forming a plurality of first polysilicon films ;

patterning said first polysilicon film to form first polysilicon strips in parallel with one another, said first polysilicon strips formed in said first direction;

forming a second gate insulating film on said first polysilicon strips

forming a second pllysilicon layer on said second gate insulating film;

patterning said second polysilicon layer, said second gate insulating film, said plurality of first polysilicon strips and said first gate insulating film to form a plurality of control gates, a plurality of second gate insulators, a plurality of floating gates, and a plurality of first gate insulators, respectively;

forming drain and source regions;

forming a first interlayer insulating layer on an entire surface of said semiconductor substrate;

forming contact-holes through said first interlayer insulating layer in alignment with said drain and source regions; and

forming a first metal wiring layeron said first interlayer insulating layer and filing said contact-holes therewith to couple said first wiring layer to a corresponding one of said drain and source regions in a memory area and a wiring layer of a logic area.

Claim 24 has been similarly amended. It is submitted that the amendments made to claims 21 and 24 removes each of the objections raised by the examiner in paragraphs 2-9 of the outstanding office action.

In paragraph 11 of the instant official action, claims 21, 22, and 24 stand rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya, et al. (U.S. Patent No. 5,838,615) (hereinafter "Kamiya") in view of Nishihara (JP 08204159) (hereinafter "Nishihara") and Kim (U.S. Patent No. 5,834,807) (hereinafter "Kim").

The rejection is respectfully traversed.

Claim 21, as amended, recites a method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors wherein the claim recites *inter alia*:

> forming a plurality of field insulating films in parallel with one another in a first direction on a semiconductor substrate, each of said plurality of field insulating films provided for a plurality of memory cell transistors and a plurality of memory transistors formed between two associated adjacent field insulating films;
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> * * * * * *
>
> patterning said first polysilicon film to form first polysilicon strips in parallel with one another, said first polysilicon strips formed in said first direction;
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> forming a second gate insulating film on said first polysilicon strips
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> forming a second pllysilicon layer on said second gate insulating film;
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> * * * * * *
>
> forming a first interlayer insulating layer on an entire surface of said semiconductor substrate;
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> * * * * * *
>
> forming a first metal wiring layer on said first interlayer insulating layer and filing said contact-holes therewith to couple said first wiring layer to a

corresponding one of said drain and source regions in a memory area and a wiring layer of a logic area.

Neither Kimaya, Nishihara nor Kim disclose or suggest the claimed invention, including the above-quoted features.

Because neither Kimaya, Nishihara nor Kim, alone or in combination, disclose or suggest the claimed invention, including the above-quoted features, the subject matter of Applicants' invention as a whole would not have been obvious at the time the invention was made to a person having ordinary skill in the art. Thus, the Patent and Trademark Office has not made out a prima facie case of obviousness under the provisions of 35 U.S.C. 103(a) and claim 21, as amended, is believed to be allowable.

Claims 22 and 23 depend directly from amended claim 21 and are, for at least this reason, believed to be allowable.

Claim 24, as amended, recites the same patentably distinct features as recited in amended claim 21 discussed above. Thus, for at least the same reasons discussed above in relation to claim 21, claim 24, as amended, is believed to be allowable.

In addition, claim 24 recites "forming aluminum backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line".

In paragraph 13 of the instant official action, the Examiner recognizes that neither Kimaya, Nishihara nor Kim disclose forming backing wiring layers. Accordingly, the Examiner cited Cacharelis et al. (U.S. Patent No. 5,550,072) (hereinafter "Cacharelis") with respect to that feature.

Cacharelis teaches that "a second metal layer 500 is deposited and patterned on the surface of second dielectric layer 480. As is evident in FIG. 21A, the patterning of metal layer 500 forms a word line 500W which extends perpendicular to bit line 470B. By means of vias 440 and 490 and tab 440T, word line 500W connects to the control gate of memory transistor 2." (See col. 5, lines 47-54.) However, Cacharelis does not teach or suggest "forming aluminum backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line", as recited in Applicants' amended claim 24.

Accordingly, even if Cacharelis could be combined with Kimaya, Nishihara and/or Kim as suggested by the Examiner, the combination would not meet the claimed

invention. Thus, the Patent and Trademark Office has not made out a prima facie case of obviousness under the provisions of 35 U.S.C. 103(a) and, for this additional reason, claim 24, as amended, is believed to be allowable.

Claim 26 now depends directly from amended claim 24 and is, for at least this reason, believed to be allowable.

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance. Reexamination and reconsideration of the application, as amended, and allowance of the claims at an early date is respectfully requested.

Respectfully submitted,

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